DATA SHEET

TDA8716
8-bit high-speed analog-to-digital converter

Product specification
Supersedes data of April 1993
File under Integrated Circuits, IC02

1996 Aug 26

Philips
Semiconductors

PHILIPS

8-bit high-speed analog-to-digital converter

TDA8716

FEATURES

- 8-bit resolution
- Sampling rate up to 120 MHz
- ECL (10 K family) compatible digital inputs and outputs
- Overflow/Underflow output
- Low power dissipation
- Low input capacitance (13 pF typ.).

GENERAL DESCRIPTION

The TDA8716 is an 8-bit high-speed Analog-to-Digital Converter (ADC) designed for HDTV and professional applications. The device converts the analog input signal into 8-bit binary coded digital words at a sampling rate of 120 MHz. All digital outputs are ECL compatible.

APPLICATIONS

- High speed analog-to-digital convertion
- Video signal digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research
- Medical systems
- Industrial instrumentation.

QUICK REFERENCE DATA

Measured over full voltage and temperature ranges, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		–5.45	–5.2	–4.95	V
V_{EED}	digital supply voltage		–5.45	–5.2	–4.95	V
I_{EEA}	analog supply current		–	50	55	mA
I_{EED}	digital supply current		–	100	110	mA
I_{EEO}	output supply current	R_L = 2.2 kΩ	–	20	25	mA
V_{RB}	reference voltage BOTTOM		–	–3.130	–	V
V_{RT}	reference voltage TOP		–	–1.870	–	V
ILE	DC integral linearity error	see Fig.8	–	±0.5	±1	LSB
DLE	DC differential linearity error	see Fig.9	–	±0.25	±0.45	LSB
EB	effective bit	f_i = 20 MHz; f_{CLK} = 100 MHz	–	7	–	bits
f_{CLK}	maximum clock frequency		120	–	–	MHz
P_{tot}	total power dissipation	excluding load	–	780	900	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8716	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101-1
TDA8716T	SO32L	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

BLOCK DIAGRAM

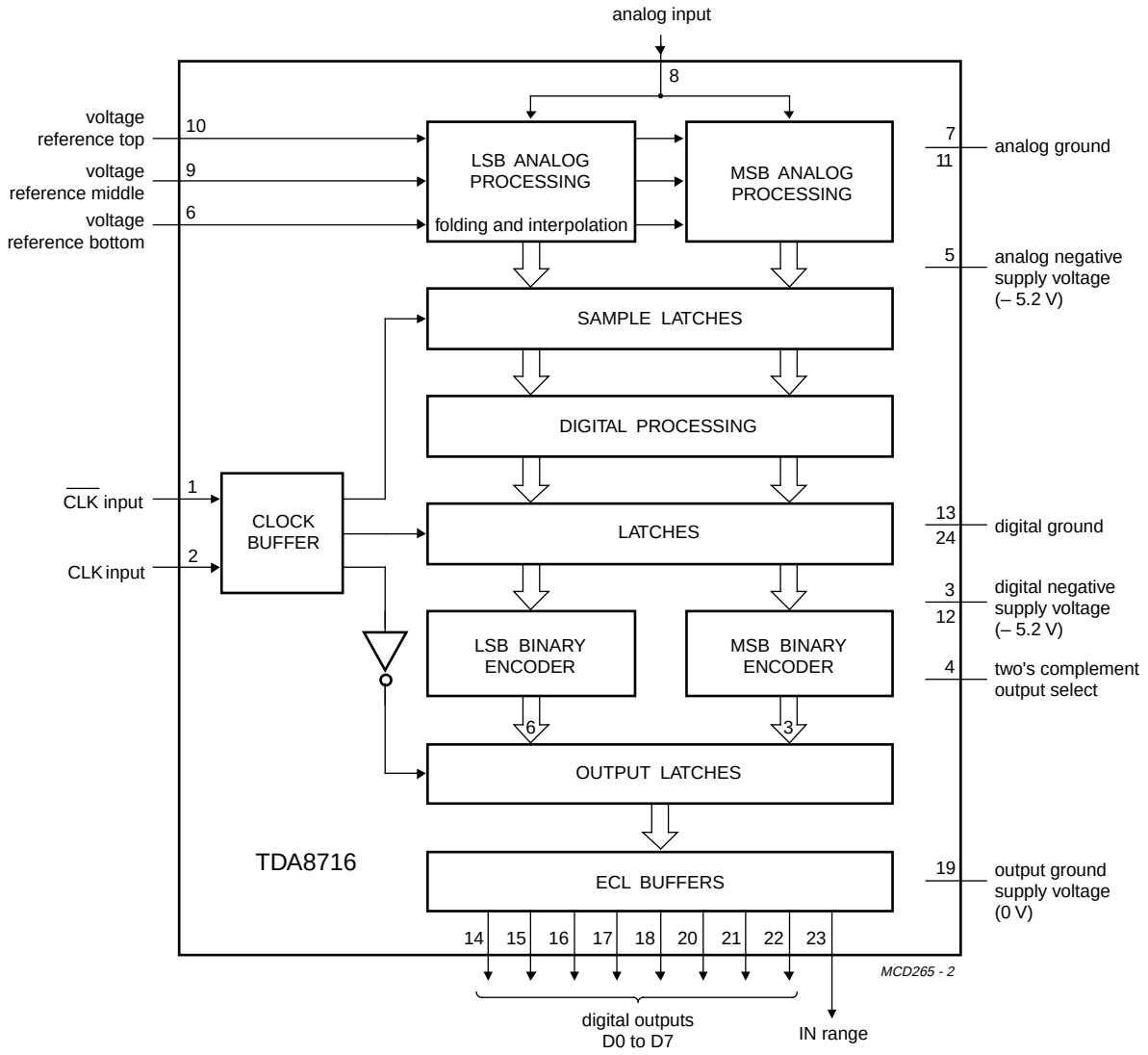


Fig.1 Block diagram; TDA8716.

PINNING TDA8716

SYMBOL	PIN	DESCRIPTION
$\overline{CLK}$	1	complementary clock input
CLK	2	clock input
V_{EED1}	3	digital negative supply voltage (–5.2 V)
C_{PLT2}	4	two's complement output select (active HIGH)
V_{EEA}	5	analog negative supply voltage (–5.2 V)
V_{RB}	6	reference voltage BOTTOM
AGND1	7	analog ground 1
V_I	8	analog input
V_{RM}	9	reference voltage MIDDLE decoupling
V_{RT}	10	reference voltage TOP
AGND2	11	analog ground 2
V_{EED2}	12	digital negative supply voltage (–5.2 V)
DGND1	13	digital ground 1
D0	14	digital output (LSB)
D1	15	digital output
D2	16	digital output
D3	17	digital output
D4	18	digital output
OGND	19	output ground supply voltage (0 V)
D5	20	digital output
D6	21	digital output
D7	22	digital output (MSB)
IR	23	IN range
DGND2	24	digital ground 2

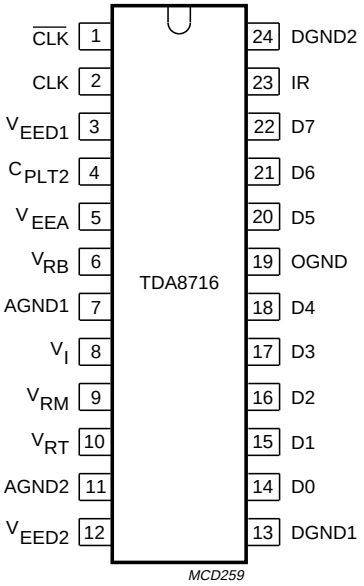


Fig.2 Pin configuration; TDA8716.

PINNING TDA8716T

SYMBOL	PIN	DESCRIPTION
$\overline{CLK}$	1	complementary clock input
CLK	2	clock input
V_{EED1}	3	digital negative supply voltage (–5.2 V)
n.c.	4	not connected
n.c.	5	not connected
C_{PLT2}	6	two's complement output select (active HIGH)
V_{EEA}	7	analog negative supply voltage (–5.2 V)
V_{RB}	8	reference voltage BOTTOM
AGND1	9	analog ground 1
V_I	10	analog input
V_{RM}	11	reference voltage MIDDLE decoupling
n.c.	12	not connected
n.c.	13	not connected
V_{RT}	14	reference voltage TOP
AGND2	15	analog ground 2
V_{EED2}	16	digital negative supply voltage (–5.2 V)
DGND1	17	digital ground 1
D0	18	digital output (LSB)
D1	19	digital output
n.c.	20	not connected
n.c.	21	not connected
D2	22	digital output
D3	23	digital output
D4	24	digital output
OGND	25	output ground supply voltage (0 V)
D5	26	digital output
D6	27	digital output
n.c.	28	not connected
n.c.	29	not connected
D7	30	digital output (MSB)
IR	31	IN range
DGND2	32	digital ground 2

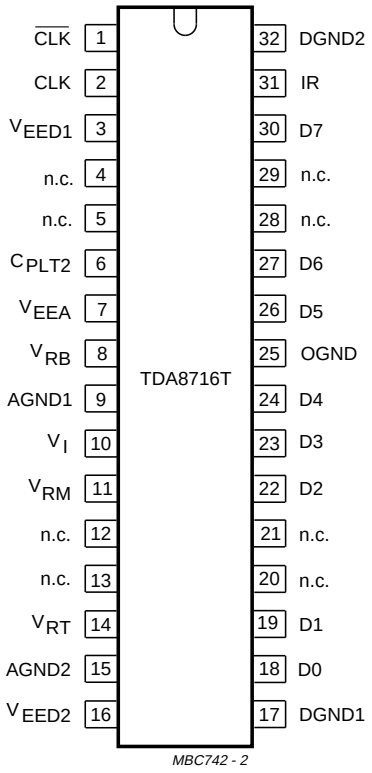


Fig.3 Pin configuration; TDA8716T.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage		–7.0	+0.3	V
V_{EED1},V_{EED2}	digital supply voltage		–7.0	+0.3	V
$V_{EEA} - V_{EED1}$; $V_{EEA} - V_{EED2}$	supply voltage differences		–1	+1	V
V_I	input voltage	referenced to AGND	V_{EEA}	0	V
$V_{CLK;\ \overline{CLK}(p\text{-}p)}$	input voltage for differential clock drive (peak-to-peak value)	note 1	–	2.0	V
I_O	output current (each output stage)		–	10	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
T_j	junction temperature		–	+150	°C

Note

1. The circuit has two clock inputs: CLK and $\overline{CLK}$. Sampling takes place on the rising edge of the clock input signal: CLK and $\overline{CLK}$ are two's complementary ECL signals.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	in free air		
	SOT101		35	K/W
	SOT287 (see Fig.4)		65	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

V_{EEA} = –4.95 to –5.45 V; V_{EED1}, V_{EED2} = –4.95 to –5.45 V; AGND, DGND and OGND shorted together; T_{amb} = 0 to +70 °C; unless otherwise specified. (Typical values taken at V_{EEA} = –5.2 V; V_{EED1}, V_{EED2} = –5.2 V; T_{amb} = 25 °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{EEA}	analog supply voltage		–5.45	–5.2	–4.95	V
V_{EED1},V_{EED2}	digital supply voltage		–5.45	–5.2	–4.95	V
I_{EEA}	analog supply current		–	50	55	mA
I_{EED1},I_{EED2}	digital supply current		–	100	110	mA
I_{EE}	output supply current	R_L = 2.2 kΩ	–	20	25	mA
V_{diff}	supply voltage differential	$V_{EEA} - V_{EED1}$; $V_{EEA} - V_{EED2}$	–0.5	0	+0.5	V
Reference voltages for the resistor ladder						
V_{RB}	reference voltage BOTTOM		–3.5	–3.13	–	V
V_{RT}	reference voltage TOP		–	–1.87	–1.5	V
V_{ref}	reference voltage differential	$V_{RT} - V_{RB}$	–	1.26	–	V
V_{OB}	voltage offset BOTTOM	note 1	–	130	–	mV
V_{OT}	voltage offset TOP	note 1	–	130	–	mV
$V_{I(p-p)}$	input voltage amplitude (peak-to-peak value)		0.95	1.0	1.5	V
I_{ref}	reference current		–	15	–	mA
R_{LAD}	resistor ladder		–	85	–	Ω
TC_{RL}	temperature coefficient of the resistor ladder		–	0.18	–	Ω/K
Inputs						
CLK and $\overline{CLK}$ input						
V_{IL}	LOW level input voltage		–1850	–1770	–1650	mV
V_{IH}	HIGH level input voltage		–960	–880	–810	mV
I_{IL}	LOW level input current	V_{CLK} = –1.77 V	–	1	–	μA
I_{IH}	HIGH level input current	V_{CLK} = –0.88 V	–	10	–	μA
R_I	input resistance		–	20	–	kΩ
C_I	input capacitance		–	2	–	pF
$V_{CLK(p-p)}$	differential clock input $V_{CLK} - V_{\overline{CLK}}$ (peak-to-peak value)		–	900	–	mV
Analog input; note 2						
I_{IB}	input current BOTTOM	V_{RB} = –3.13 V	–	0	–	μA
I_{IT}	input current TOP	V_{RT} = –1.87 V	–	170	–	μA
R_I	input resistance		–	7	–	kΩ
C_I	input capacitance		–	13	20	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs (R_L = 2.2 kΩ)						
Digital 10K ECL outputs (D0 to D7; IR)						
V_{OL}	LOW level output voltage		–1850	–1770	–1600	mV
V_{OH}	HIGH level output voltage		–960	–880	–810	mV
I_{OL}	LOW level output current		–	1.8	4.0	mA
I_{OH}	HIGH level output current		–	2.0	4.0	mA
Timing (f_{CLK} = 100 MHz; R_L = 2.2 kΩ; see Fig.5**)**						
t_{ds}	sampling delay		–	1	3	ns
t_{HD}	output hold time		4	–	–	ns
t_d	output delay time	note 3				
		C_L = 3.3 pF	–	–	7.5	ns
		C_L = 7.5 pF	–	–	9	ns
t_{aj}	aperture jitter		–	15	–	ps
Switching characteristics						
f_{CLK}; $f_{\overline{CLK}}$	maximum clock frequency		120	–	–	MHz
Analog signal processing (f_{CLK} = 100 MHz)						
G_{diff}	differential gain	note 4	–	0.3	–	%
ϕ_{diff}	differential phase	note 4	–	0.4	–	°C
Harmonics (full scale); f_i = 10 MHz; f_{CLK} = 100 MHz						
f1	fundamental		–	0	–	dB
f2	even harmonics		–	–60	–	dB
f3	odd harmonics		–	–50	–	dB
Transfer function						
ILE	DC integral linearity error		–	±0.5	±1	LSB
DLE	DC differential linearity error		–	±0.25	±0.45	LSB
AILE	AC integral linearity error	note 4	–	±1	±1.5	LSB
EB	effective bits	Figs 13 and 14; note 5; f_{CLK} = 100 MHz				
	f_i = 4.43 MHz	see Fig.10	–	7.7	–	bits
	f_i = 10 MHz	see Fig.11	–	7.5	–	bits
	f_i = 20 MHz	see Fig.12	–	7.0	–	bits
	f_i = 30 MHz		–	6.5	–	bits
BER	bit error rate	f_{CLK} = 100 MHz; f_i = 10 MHz; V_i = ±8 LSB at code 128; 50% clock duty factor	–	10^{-11}	–	times/ samples

Notes

1. Voltage offset BOTTOM (V_{OB}) is the difference between the analog input which produces data outputs equal to 00 and the reference voltage BOTTOM (V_{RB}), at T_{amb} = 25 °C. Voltage offset TOP (V_{OT}) is the difference between reference voltage TOP (V_{RT}) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.
2. The analog input is not internally biased. It should be externally biased between V_{RB} and V_{RT} levels.
3. The TDA8716 can only withstand one or two 10K or 100K ECL loads in order to work-out timings at the maximum sampling frequency. It is therefore recommended to minimize the printed-circuit board load by implementing the load device as close as possible to the TDA8716.
4. Full-scale sinewave; f_i = 4.43 MHz; f_{CLK}, $f_{\overline{CLK}}$ = 100 MHz.
5. Effective bits are obtained via a Fast Fourier Transformer (FFT) treatment taking 4 K acquisition points per period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to SNR: SNR = EB (dB) × 6.02 + 1.76.

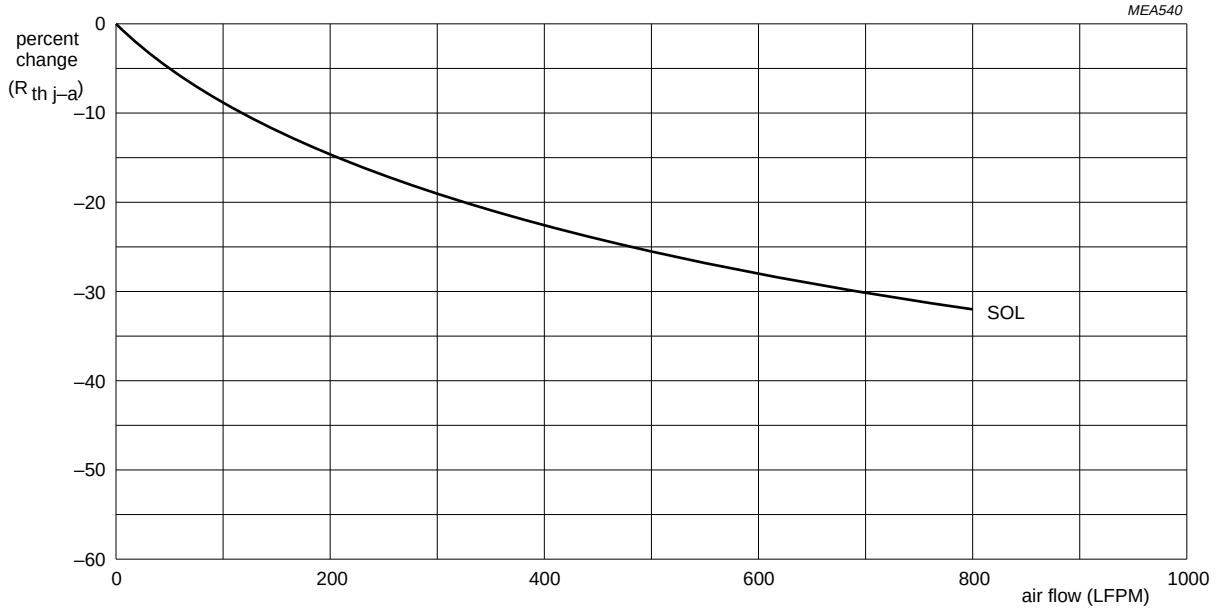


Fig.4 Average effect of air flow on thermal resistance.

Table 1 Output coding (CPLT2 HIGH)

STEP	V_I (TYP.)	BINARY OUTPUTS D7 to D0	IR
Underflow	< –3 V	00000000	0
0	–3 V	00000000	1
1	.	00000001	1
.	.	.....	.
.	.	.....	.
.	.	.....	.
254	.	11111110	1
255	–2 V	11111111	1
Overflow	> –2 V	11111111	0

Table 2 Two's complement coding

C_{PLT2}	D7 (MSB)
1 (V_{IH})	non inverted
0 (V_{IL})	inverted

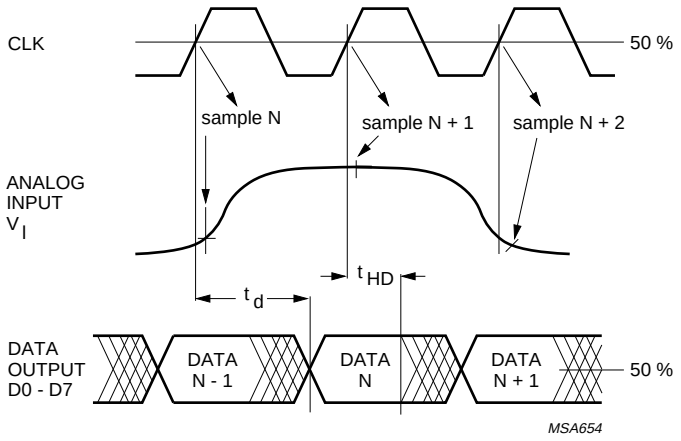
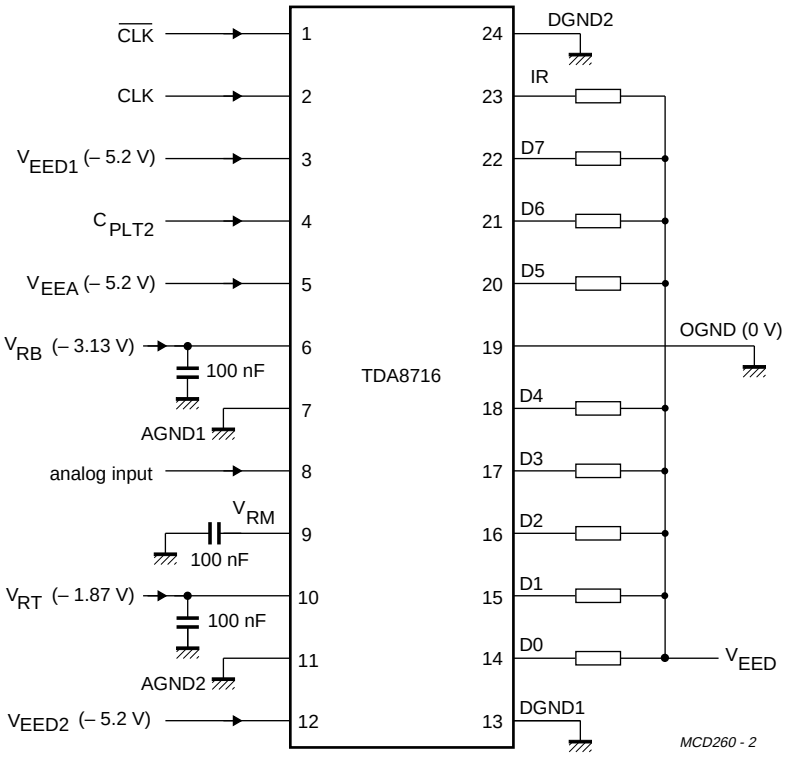


Fig.5 Timing diagram.

APPLICATION INFORMATION

Additional application information will be supplied upon request, please quote reference number FTV/AN 9109.



Typical value for resistors = 2.2 kΩ.

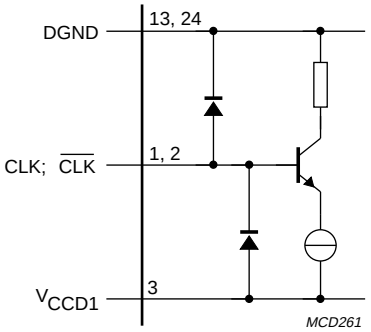
Lower resistor values can be used down to 500 Ω to obtain higher sampling frequencies in the 150 MSPS range (limited by t_d and t_{HD} timings). In this configuration a DC shift of the ECL output levels V_{OL} and V_{OH} will occur.

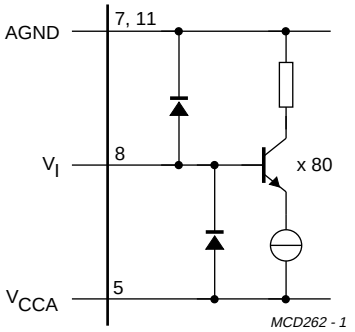
V_{RB}, V_{RT} and V_M are decoupled to AGND.

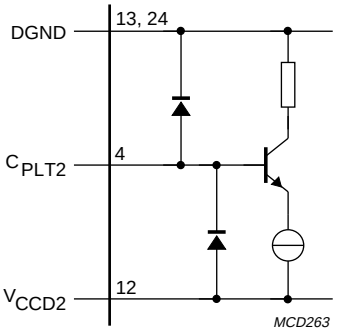
Analog, digital and output supplies should be separated and decoupled.

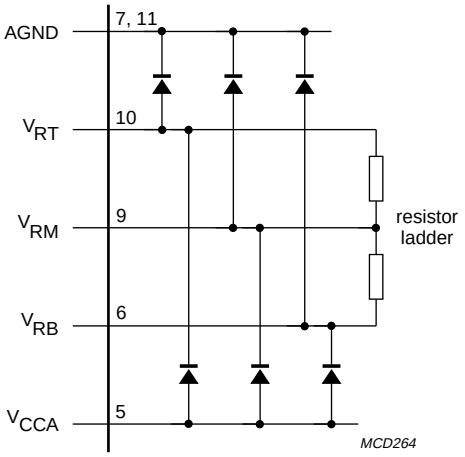
The external voltage regulator must be constructed in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value.

Fig.6 Application diagram; TDA8716.









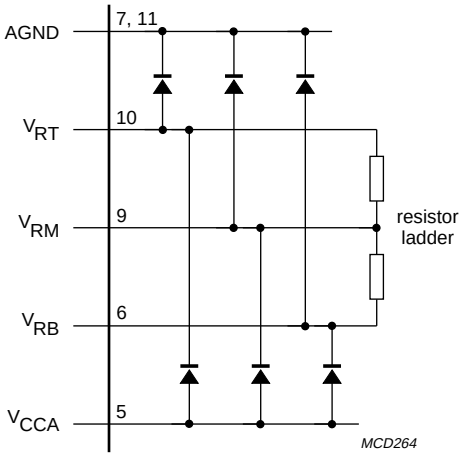


Fig.7 Internal pin configuration diagram.

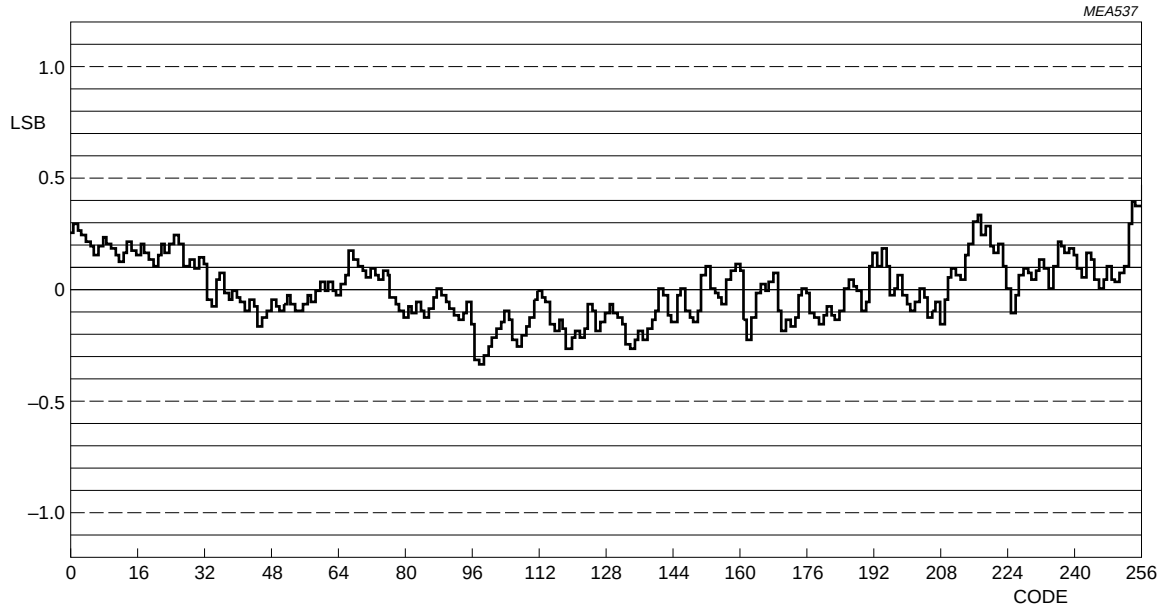


Fig.8 DC Integral Linearity Error (ILE).

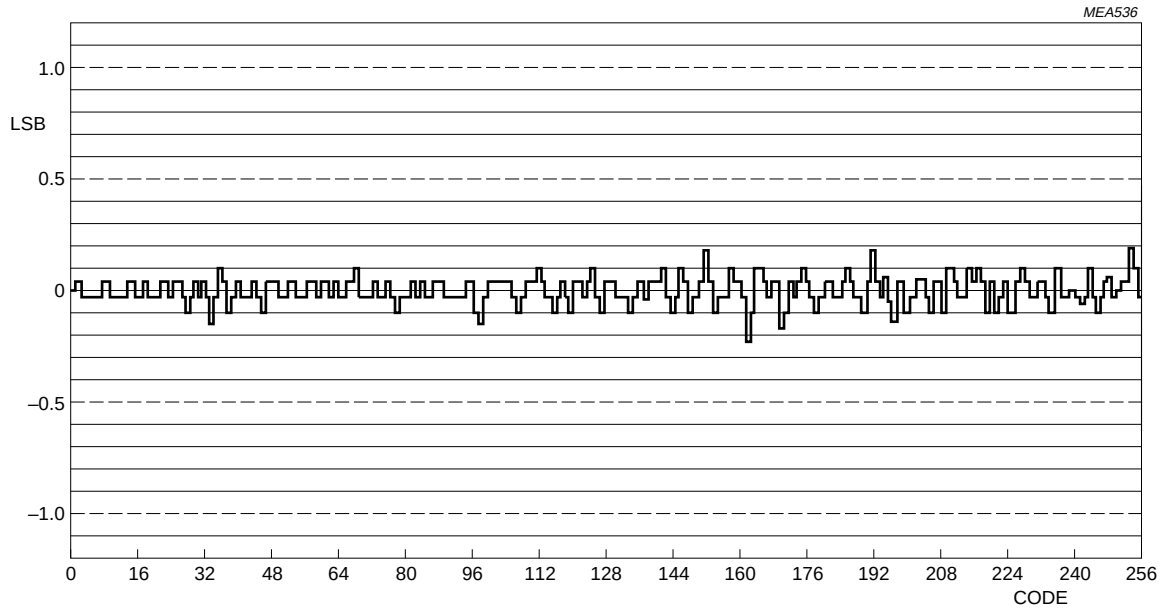
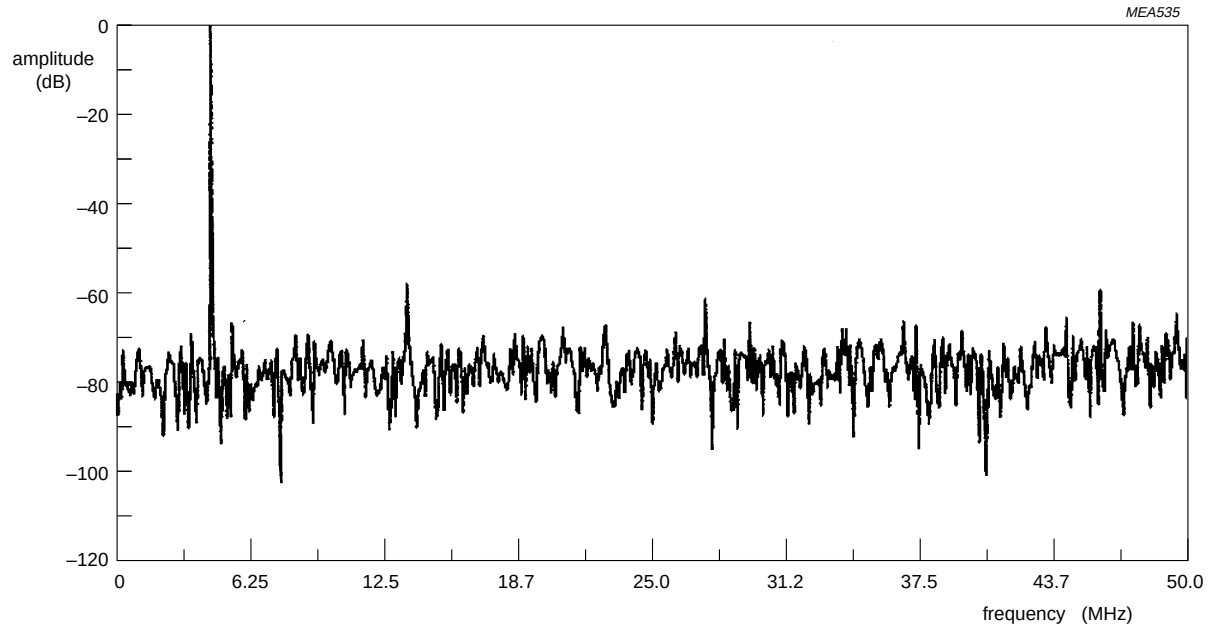
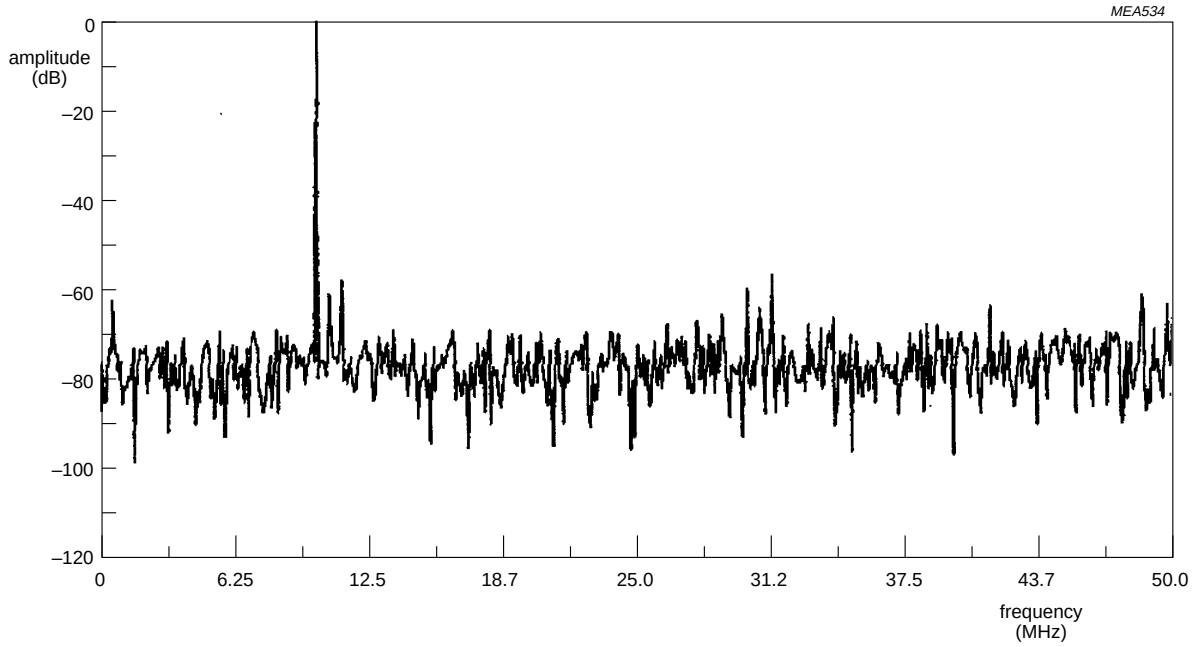


Fig.9 DC Differential Linearity Error (DLE).



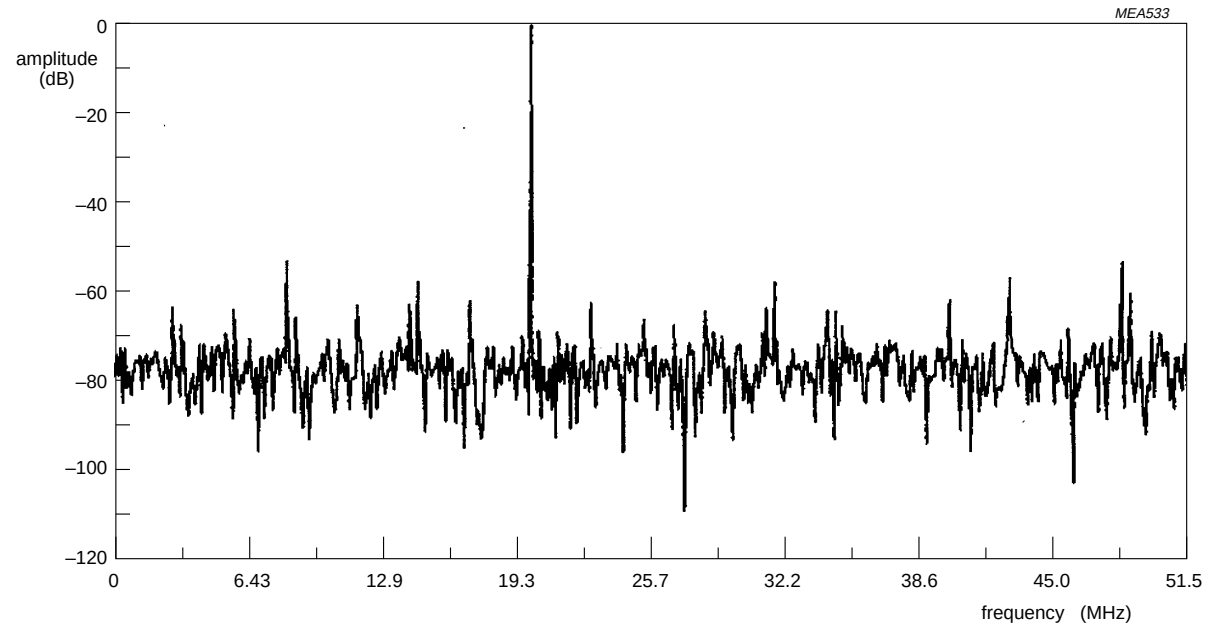
Effective bits: 7.74; Harmonic levels (in dB): 2nd = –69.34; 3rd = –58.85; 4th = –82.55; 5th = –68.16 and 6th = –63.01.

Fig.10 Fast fourier transformer (f_{CLK} = 100 MHz; f_i = 4.43 MHz).



Effective bits: 7.57; Harmonic levels (in dB): 2nd = –82.07; 3rd = –61.90; 4th = –75.70; 5th = –65.61 and 6th = –72.50.

Fig.11 Fast fourier transformer (f_{CLK} = 100 MHz; f_i = 10 MHz).



Effective bits: 7.04; Harmonic levels (in dB): 2nd = –61.36; 3rd = –56.66; 4th = –61.97; 5th = –62.79 and 6th = –61.52.

Fig.12 Fast fourier transformer (f_{CLK} = 100 MHz; f_i = 20 MHz).

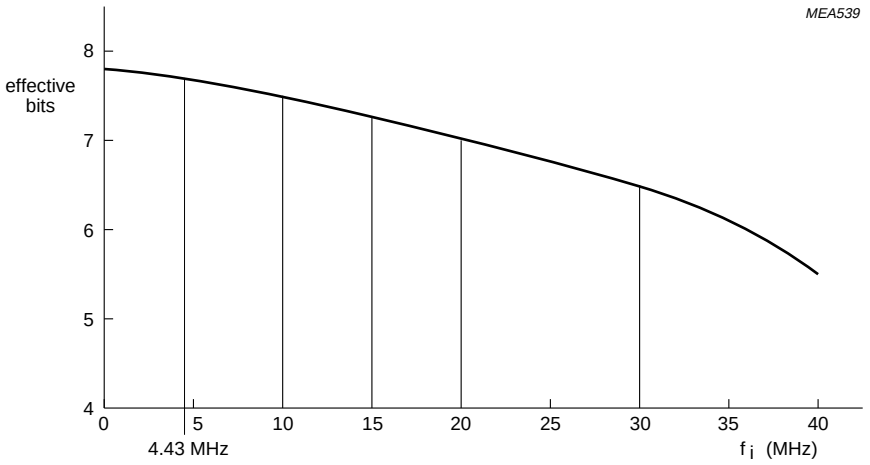


Fig.13 Typical effective bit as a function of input signal at f_{CLK} = 100 MHz.

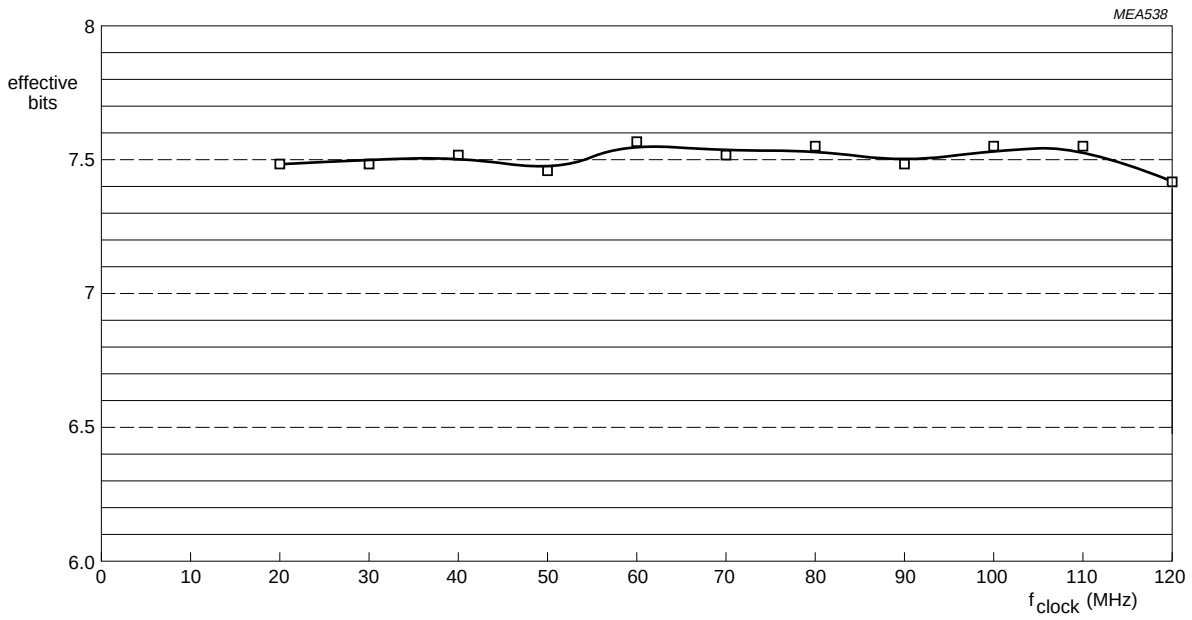
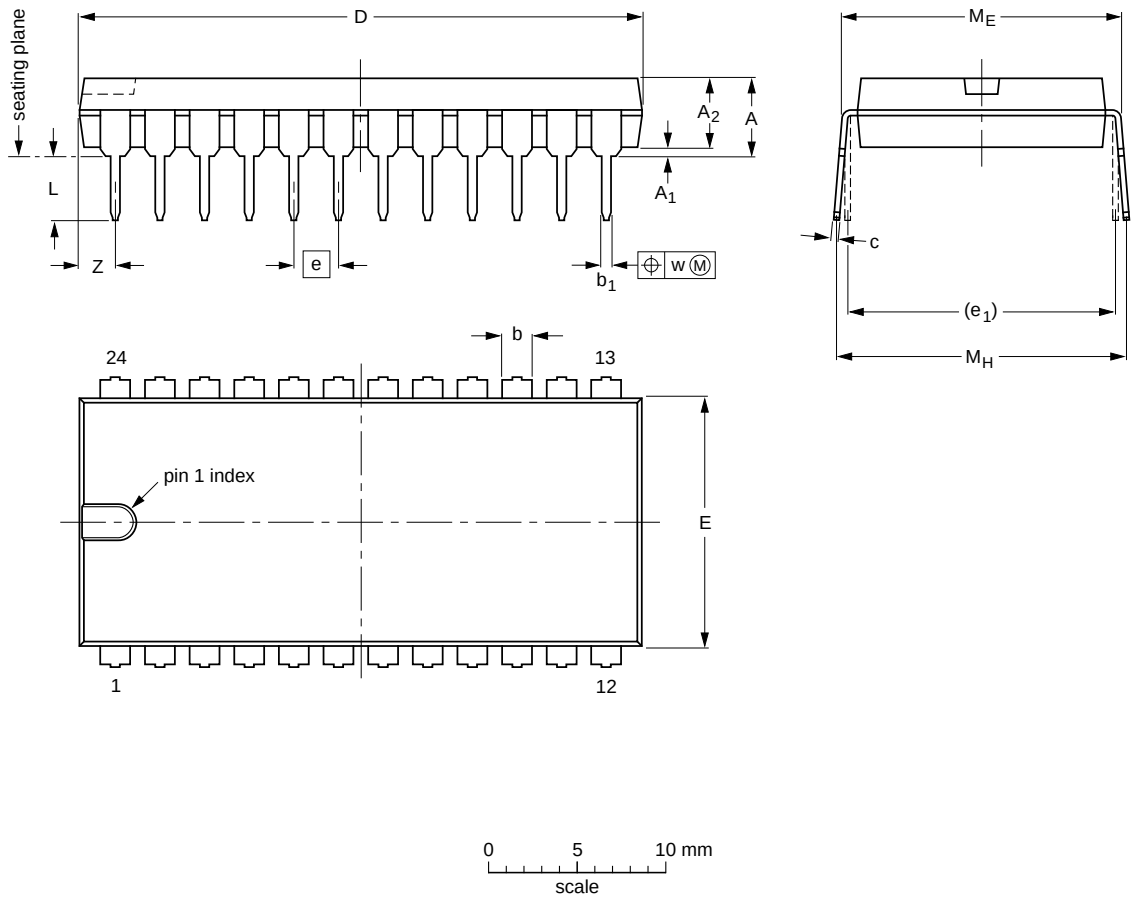


Fig.14 Typical effective bits as a function of clock frequency at f_i = 10 MHz.

PACKAGE OUTLINES

DIP24: plastic dual in-line package; 24 leads (600 mil) **SOT101-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

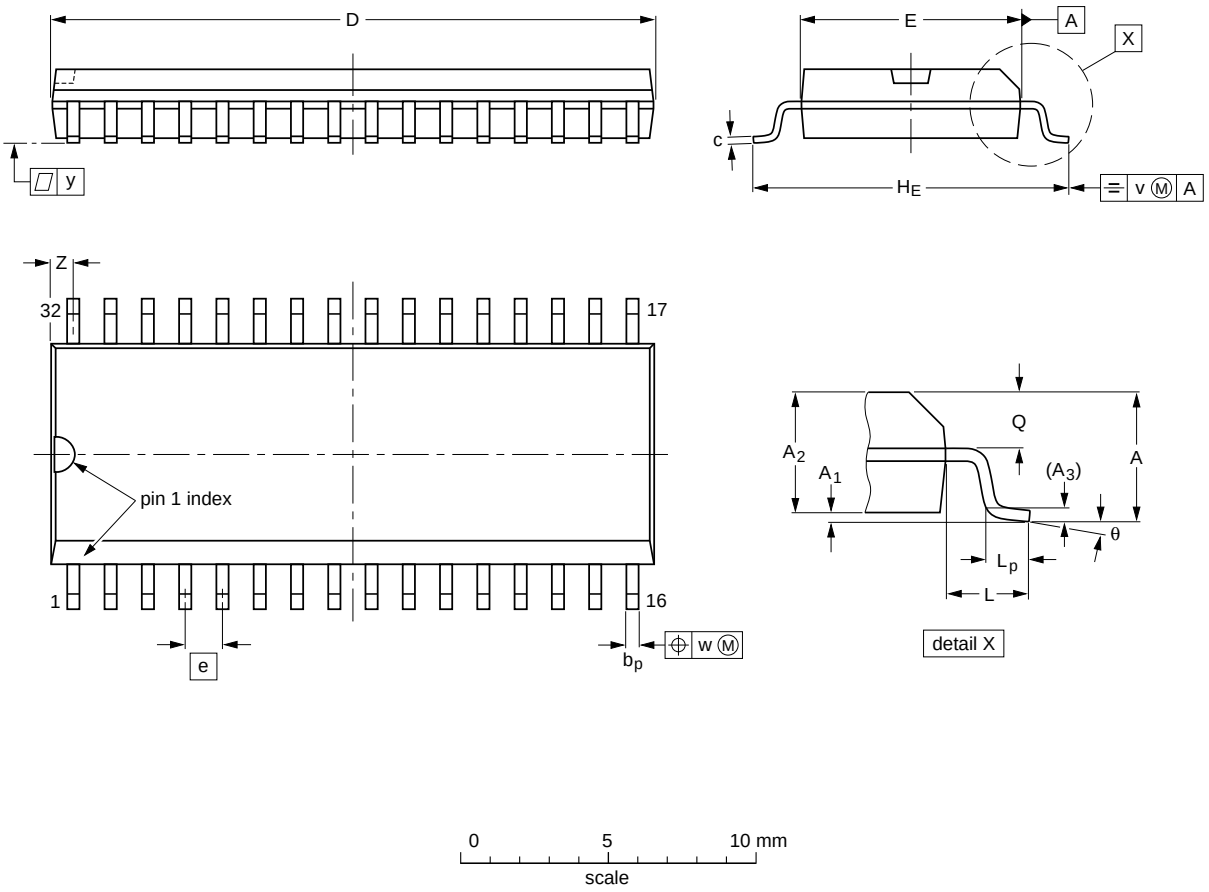
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT101-1	051G02	MO-015AD				~~92-11-17~~ 95-01-23

SO32: plastic small outline package; 32 leads; body width 7.5 mm **SOT287-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.086	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT287-1						~~92-11-17~~ 95-01-25

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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